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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,956	01/29/2004	Kenji Funamoto	5-130US-FF	2333

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MCGINN INTELLECTUAL PROPERTY LAW GROUP, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

EXAMINER	
STIGLIC, RYAN M	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,956	FUNAMOTO, KENJI	
	Examiner	Art Unit	
	Ryan M. Stiglic	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-4 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 29 January 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4 are pending and have been examined.

2. Claims 1-4 are rejected.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Gelke et al. (US006735661B2).

For claim 1 Gelke discloses:

A memory device comprising (Fig. 1):

- a data memory (Fig. 1, 1; col. 2, ll. 47-59) to and from which data is input and output via a data bus (Fig. 1, 'Flash bus' 2; col. 2, ll. 47-59) for a data memory; and

- a plurality of buffer circuits (Fig. 1, 4; col. 2, ll. 47-59) for inputting and outputting data to and from said data memory via a first data bus (The Examiner has interpreted the first data bus as being the 'data bus' from the first limitation since nothing in the claim precludes such a structure; Fig. 1, 'Flash bus'; col. 2, ll. 47-59; col. 3, line 62 – col. 4, line 5) that has a bus width the same as that of the data bus for said data memory and that is electrically connected to the data bus for said data memory (col. 2, ll. 47-59; col. 3, line 62 – col. 4, line 5), and inputting and outputting data to and from a data processing circuit via a second data bus having a bus width smaller than that of the data bus for said data memory (col. 2, ll. 47-59; col. 3, line 62 – col. 4, line 5).

For claim 3 Gelke discloses:

The device according to claim 1, wherein the bus width of the second data bus is a fraction of that of the bus for said data memory (col. 2, ll. 47-59; col. 3, line 62 – col. 4, line 5).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muramatsu et al. (US006384832B1) as applied to claim 1 above, and further in view of Gelke et al.

Muramatsu teaches an image processing apparatus that comprises an arbitration circuit (Fig. 6, 20; col. 7, ll. 38-60) for controlling the plurality of buffer circuits (Fig. 6, items 100,110,120,130,140,150) in such a manner that image data representing images of different frames is input and output to and from different buffer circuits (col. 7, line 38 – col. 8, line 25) in a common time period (col. 8, ll. 6-7). Furthermore Muramatsu teaches the arbitration circuit (Fig. 6, 20) also acts a selector, which is connected between said plurality of buffer circuits and said data memory, for allowing input/output of data between any one of said plurality of buffer circuits and said data memory (col. 7, line 38 – col. 8, line 25). Muramatsu however fails to teach an image processing apparatus (including memory) comprising a first data bus that has a width greater then a second data bus that connects to a processing circuit.

Gelke teaches a processing circuit (Fig. 1, 3) connected to a plurality of buffers via a second data bus with a bus width of n bits (col. 2, ll. 47-59; col. 3, line 62 – col. 4, line 5). Gelke further teaches a flash memory is connected to a plurality of buffers via a first data bus that is of bus width m (where m is greater than n) (col. 2, ll. 47-59; col. 3, line 62 – col. 4, line 5).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to provide a first data bus connecting buffer circuits to memory with a bus width larger than the bus width of a second data bus connected to a processing circuit such that the processing circuit can now fetch a word of data at time from the memory without using consecutive processor fetch cycles (Gelke; col. 2, ll. 6-15).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure since it pertains to the transfer of image data and systems with varying bus widths to increase system performance.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

RMS